WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, comprising:

forming a lower interconnect on a semiconductor substrate;

forming an dielectric film on said lower interconnect;

performing selective etching on said dielectric film to form a via hole that reaches the proximity of said lower interconnect;

forming an anti-reflection coating at a bottom portion of said via hole;

forming a resist layer over the substrate so as to substantially fill a space remaining on said anti-reflection coating in said via hole;

forming an opening in said resist layer;

performing selective etching on said dielectric film utilizing said resist layer as a mask to form an interconnect trench for connection with said via hole;

removing said resist layer and said anti-reflection coating in said via hole to have an upper surface of said lower interconnect exposed; and

substantially filling said via hole and said interconnect trench with a metal layer;

wherein said anti-reflection coating is formed to have its thickness at a central portion of said via hole thinner than a

distance between the upper surface of said lower interconnect and a bottom portion of said interconnect trench in said forming said anti-reflection coating.

2. The method as set forth in Claim 1, further comprising removing said anti-reflection coating remaining at a sidewall of said via hole, between said forming an opening in said resist layer and said forming said interconnect trench.

3. The method as set forth in Claim 1, wherein a material and a forming condition of said anti-reflection coating and said resist layer are selected in such a manner that an etching rate of said anti-reflection coating becomes slower than an etching rate of said resist layer in said performing etching on said dielectric film to form said interconnect trench.

4. The method as set forth in Claim 2, wherein a material and a forming condition of said anti-reflection coating and said resist layer are selected in such a manner that an etching rate of said anti-reflection coating becomes slower than an etching rate of said resist layer in said performing etching on said dielectric film to form said interconnect trench.

5. A method of manufacturing a semiconductor device, comprising:

forming a lower interconnect on a semiconductor substrate;

forming an dielectric film on said lower interconnect;

performing selective etching on said dielectric film to form a via hole that reaches the proximity of said lower

interconnect;

forming an anti-reflection coating at a bottom portion of said via hole;

forming a resist layer over the substrate so as to substantially fill a space remaining on said anti-reflection coating in said via hole;

forming an opening in said resist layer;

performing selective etching on said dielectric film utilizing said resist layer as a mask to form an interconnect trench for connection with said via hole;

removing said resist layer and said anti-reflection coating in said via hole to have an upper surface of said lower interconnect exposed; and

substantially filling said via hole and said interconnect trench with a metal layer;

wherein said interconnect trench is formed with said anti-reflection coating formed in said via hole being covered with said resist layer in said forming said interconnect trench.

6. The method as set forth in Claim 5, wherein a material and a forming condition of said anti-reflection coating and said resist layer are selected in such a manner that an etching rate of said anti-reflection coating becomes slower than an etching rate of said resist layer in said performing etching on said dielectric film to form said interconnect trench.

7. The method as set forth in Claim 5, further comprising

removing said anti-reflection coating remaining at a sidewall of said via hole, between said forming an opening in said resist layer and said forming said interconnect trench.

8. The method as set forth in Claim 7, wherein a material and a forming condition of said anti-reflection coating and said resist layer are selected in such a manner that an etching rate of said anti-reflection coating becomes slower than an etching rate of said resist layer in said performing etching on said dielectric film to form said interconnect trench.

9. A method of manufacturing a semiconductor device, comprising:

forming a lower interconnect on a semiconductor substrate;

forming an dielectric film on said lower interconnect;

performing selective etching on said dielectric film to form a via hole that reaches the proximity of said lower interconnect;

forming an anti-reflection coating at a bottom portion of said via hole;

forming a resist layer over the substrate so as to substantially fill a space remaining in said via hole;

forming an opening in said resist layer;

performing selective etching on said dielectric film utilizing said resist layer as a mask to form an interconnect trench for connection with said via hole;

removing said resist layer and said anti-reflection

coating in said via hole; and

substantially filling said via hole and said interconnect trench with a metal layer;

wherein a material and a forming condition of said anti-reflection coating and said resist layer are selected in such a manner that an etching rate of said anti-reflection coating becomes faster than an etching rate of said resist layer in said performing etching on said dielectric film to form said interconnect trench, and

said anti-reflection coating is formed to have its thickness at a central portion of said via hole greater than a distance between the upper surface of said lower interconnect and a bottom portion of said interconnect trench in said forming said anti-reflection coating.